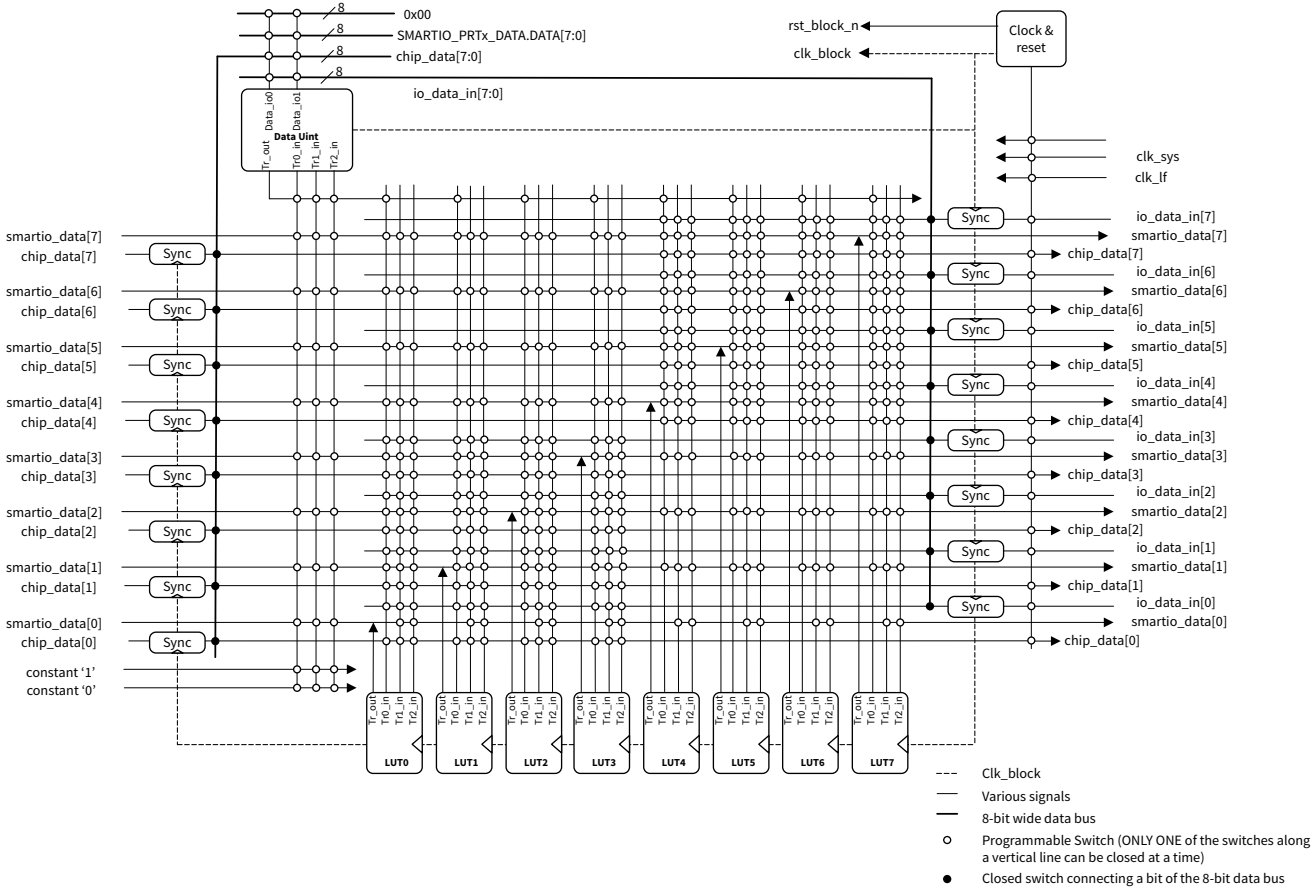
0x00
SMARTIO_PRTx_DATA.DATA[7:0]
chip_data[7:0]
io_data_in[7:0]
rst_block_n
clk_block
Clock & reset
Data Uint
Tr_out
data_io0
data_io1
Tr0_in
Tr1_in
Tr2_in
clk_sys
clk_lf
Sync
smartio_data[7]
chip_data[7]
smartio_data[6]
chip_data[6]
smartio_data[5]
chip_data[5]
smartio_data[4]
chip_data[4]
smartio_data[3]
chip_data[3]
smartio_data[2]
chip_data[2]
smartio_data[1]
chip_data[1]
smartio_data[0]
chip_data[0]
io_data_in[7]
io_data_in[6]
io_data_in[5]
io_data_in[4]
io_data_in[3]
io_data_in[2]
io_data_in[1]
io_data_in[0]
constant '1'
constant '0'
LUT0
LUT1
LUT2
LUT3
LUT4
LUT5
LUT6
LUT7
Clk_block
Various signals
8-bit wide data bus
Programmable Switch (ONLY ONE of the switches along a vertical line can be closed at a time)
Closed switch connecting a bit of the 8-bit data bus